

CLAIMS

1 1. A method comprising:
2 loading a value into a register of a memory device;
3 generating a test sequence in response to the value in the register during a self-test mode
4 of operation of the memory device;
5 testing the memory device with the test sequence; and
6 storing a signature as a result of the test sequence into a shift register.

1 2. The method of claim 1 wherein the value is a four bit field.

1 3. The method of claim 1 wherein the memory device is a polymer memory organized as a
2 8K by 8K array with a 256 bit data word during the self-test mode of operation.

1 4. The method of claim 1 wherein the test sequence is one of a test pattern or a plurality of
2 test patterns.

1 5. An article comprising:
2 a storage medium having a plurality of machine readable instructions, wherein when the
3 instructions are executed by a memory device, the instructions provide to:
4 load a value into a register of the memory device;
5 generate a test sequence in response to the value in the register during a self-test mode of
6 operation of the memory device;
7 test the memory device with the test sequence;

8 store a signature as a result of the test sequence into a shift register.

1 6. The article of claim 5 wherein the value is a four bit field.

1 7. The article of claim 5 wherein the memory device is a polymer memory organized as a
2 8K by 8K array with a 256 bit data word during the self-test mode of operation.

1 8. The article of claim 5 wherein the test sequence is one of a test pattern or a plurality of
2 test patterns.

1 9. An apparatus to test a memory device comprising:
2 a register integrated within the memory device to load a value;
3 a logic to generate a test sequence in response to the value during a self-test mode of
4 operation of the memory device and to test the memory device with the test sequence ;
5 a shift register to store a signature as a result of the test sequence; and
6 an error counter to tabulate the number of errors as the result of the test sequence.

1 10. The apparatus of claim 9 wherein the value is a four bit field.

1 11. The apparatus of claim 9 wherein the memory device is a polymer memory organized as
2 a 8K by 8K array with a 256 bit data word during the self-test mode of operation.

1 12. The apparatus of claim 9 wherein the test sequence is one of a test pattern or a plurality of
2 test patterns.

1 13. The apparatus of claim 9 wherein the error counter utilizes a shift register to tabulate the
2 number of errors.

1 14. A memory device comprising:
2 a logic to support programmable built-in self-test (BIST) patterns; and
3 an error counter to tabulate a number of errors detected as a result of
4 at least one BIST pattern applied to the memory device.

1 15. The memory device of claim 14 further comprising a plurality of programmable input
2 data to
3 test the memory device.

1 16. The memory device of claim 14 wherein at least one BIST pattern is to be generated by a
2 data pattern stored in a chip test data register based at least in part on an address of the memory.

1 17. The memory device of claim 14 wherein the error counter is reset to zero before the BIST
2 pattern is applied to the memory device.

1 18. The memory device of claim 14 wherein the error counter is incremented if the errors
2 exceed a programmable threshold for an address of the memory device.

- 1 19. The memory device of claim 14 wherein the error counter is to count errors for a subset of
2 the memory device, defined by a starting address and an ending address.
- 1 20. The memory device of claim 14 wherein the error counter is to count errors for a subset of a
2 word, which represents a number of bits in an address.
- 1 21. The memory device of claim 14 wherein the error counter is a plurality of registers, the
2 registers to store a count for at least one defect type and to store a count of the number of good
3 bits for an address of the memory device.
- 1 22. The memory device of claim 21 wherein the defect type is either one of a stuck at one fault
2 or a stuck at zero fault.